49 78. The semiconductor memory according to claim 46, wherein the voltage generator circuit includes a first circuit and a second circuit, the current supply capability of the first circuit being greater than that of the second circuit, the first circuit being operative in response to selection of one of said plurality of word lines.

Cont. 2 D2

REMARKS

With entry of this amendment, claims 21-22 and 34-76 remain in this application. Claims 21-28 were previously allowed. Although claims 21 and 22 were allowed, they have been amended, to better define over the prior art references submitted March 7 and April 4, 1997. New claims 34-72 have been added. These claims have been drafted to distinguish over the art previously cited by the Examiner and that newly cited by Applicants.

The Examiner had previously rejected claims over Takemae and Gupta.

Claim 34 as now presented clearly distinguishes over this art, in claiming that the voltage generator circuit produces a first voltage larger than the operating voltage both when no word line of the plurality of word lines is selected and when a word line is selected. This is a feature that is found in all of the claims now presented. Takemae does not disclose any specific techniques of a boosting circuit for word lines and does not disclose that a boosted voltage is generated when the word lines are not selected. Therefore, there is no basis for the Examiner alleging that the claimed invention would be obvious over this cited reference, which in no manner describes a word line drive circuit.

The Examiner's second reference to Gupta discloses an on-chip charge pump boost circuit and an EEPROM. However, what it shows in Fig. 3B is that a power supply voltage

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of 5 volts is applied directly after selection of the word line and then the word voltage is progressively increased or boosted by the charge pump circuit. In other words, Gupta does not disclose that a boosted voltage is generated when no word lines are selected. Nor is there any suggestion in either of the references which would lead to doing this. Writing into the EEPROM in Gupta is performed by controlling a threshold voltage of a memory cell transistor for a time interval for which a high voltage is applied to word lines; this is a relatively long time on the order of a few milliseconds. Accordingly, the timing at which a voltage is supplied to the word line is not a teaching that one can find in this disclosure related to an EEPROM. Thus, neither Gupta alone nor in combination with Takemae suggest this feature.

THE TEACHING OF THE REFERENCES SUBMITTED ON DECEMBER 12, 1996 AND APRIL 4, 1997

JP-A-59-38996 (Laid Open On March 3, 1984

This publication relates to a DRAM word line drive circuit. The conventional boosting circuit in Fig. 3 describes a self-boost type voltage boosting circuit which includes a word line drive signal ϕw generating circuit 30, a boost signal ϕp generating circuit 31, boosting capacitance 33 and a parasitic capacitance 34. Fig. 5 shows a word line drive boosting circuit which includes an additional charge pump boosting circuit in parallel with additionally the self-boosted voltage generating circuit of Fig. 3. The charge pump boosting circuit includes a switching FET 36, a rectifying FET 41, a charging FET 40 and a boosting capacitance 38. The object of the invention in this reference is to prevent a voltage drop during selection of a word line which continues for a long time by using the additional boosting circuit, since the self-boosting circuit cannot provide a long-term boosted voltage.

Figs. 4 and 6 are waveform diagrams which show that a self-boost voltage generating circuit and an additional charge pump type boost circuit are operated only when a word line is selected.

JP-A-59-201464 (Laid Open On November 15, 1984)

This reference relates to a DRAM having a memory cell (Fig. 1) which includes a P-MOS transistor and a capacitor. A word line driving circuit is disclosed in Fig. 4 and the potential of the word line WLi is controlled as below, which is shown at the lowermost of Fig. 5: When a memory cell is not selected, the word line WLi is fixed at the power supply voltage Bcc; and when the memory cell is selected, at step 1 (read operation), the word line WLi is once driven to a potential Vss+$|$VTP$|$, which is higher than Vss by a threshold voltage $|$VTP$|$ from Vcc; and at step 2 (write operation or rewrite operation), the signal ϕWL is turned on after a predetermined time elapses from the condition of the step 1, whereby the word line WLi is further driven to a substrate potential VBB which is a negative potential. The substrate voltage VBB generation circuit generating a negative potential is formed of a charge pump circuit which is constantly driven by an oscillation circuit as shown in Fig. 3. The substrate voltage VBB is constantly generated, is applied to a semiconductor substrate as a bias voltage and is utilized for the above-mentioned step 2 upon selection of word line WLi as well.

JP-A-60-69896 (Laid Open On April 20, 1985)

This reference discloses reduction of the power consumption of a substrate voltage generation circuit formed of a charge pump circuit which is mounted on a DRAM. More specifically, the substrate voltage generation circuit is comprised of a first charge pump section (13 in Fig. 3) which is constantly driven by a self-excited oscillator 11 to generate a

substrate voltage Vbb of a relatively small current supply capability and a second charge pump section (15 in Fig. 3) which is selectively enabled by a RAS signal (i.e. row address strobe signal) during an active operation of the DRAM (i.e. in memory access).

JP-A-59-213090 (Laid Open On December 1, 1984)

This reference discloses a dynamic random access memory (DRAM) in which a word line drive circuit (Fig. 3) is controlled by a small-amplitude signal Rc (an amplitude of 0-3V) and an external supply voltage VDD1 (5V) is applied to the word line at a single stage (Fig. 4). Fig. 1 shows a self-boosted word line drive circuit of the conventional type by which the background of that invention is explained. Fig. 2 shows that a voltage of about 7 volts is applied to the word line when the external supply voltage is 5 volts.

JP-A-58-185091 (Laid Open On October 28, 1983)

This reference discloses a word line drive circuit and a decode circuit for a DRAM in which a supply voltage Vc is applied to a word line by applying a voltage higher than the supply voltage Vc to the gate of an N-type MOS transistor, for example, the supply voltage Vc is applied to the word line WL1 via transistors 254, and 571. In this case, a voltage higher than the supply voltage Vc is applied to the transistors 254 and 571 from the decode circuits 100 and 300 whereby the voltage drop due to the N-type MOS transistors 254 and 571 is prevented.

Figs. 5 and 7 show specific circuits for the decode circuits 100 and 300, which have self-boosting circuits, respectively, as their main structure (as shown by the fundamental circuit in Fig. 1(C)). Figs. 2-4 and 6 show modifications of the drive circuit except the decode section. The modifications also include self-boosting circuits as their essential structure.

Figs. 8 and 9 disclose a boosting circuit which constantly generates boosted voltages VHa, VHb which are higher than a supply voltage Vc, by periodical pulses $\phi 1$ and $\phi 2$. The circuits in Figs. 2 to 7 have a self-boosting structure as their main element, so that a voltage generated by the self-boosting circuit attenuates with time. To prevent the lowering of the boosted voltage with time the voltages VHa, VHb are used to hold the boosted voltage which is once generated by the self-boosting circuit.

As noted previously, the claims not presented have been written to define over all of these references. Thus, the newly presented claims distinguish over the art and are in condition for allowance, prompt notice of which is respectfully solicited.

Authorization is hereby granted to charge the fee of $770.00 to Deposit Account No. 11-0600.

The Office is also hereby authorized to charge any additional fees or credit any overpayment under 37 CFR § 1.17(r) to Kenyon & Kenyon Deposit Account No. 11-0600.

The Office is invited to contact the undersigned at (202) 429-1776 to discuss any matter concerning this Application.

Respectfully submitted,

Dated: 5 June 1997

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